METHOD FOR MANUFACTURING THREE-DIMENSIONAL STACKED CHIP PACKAGE

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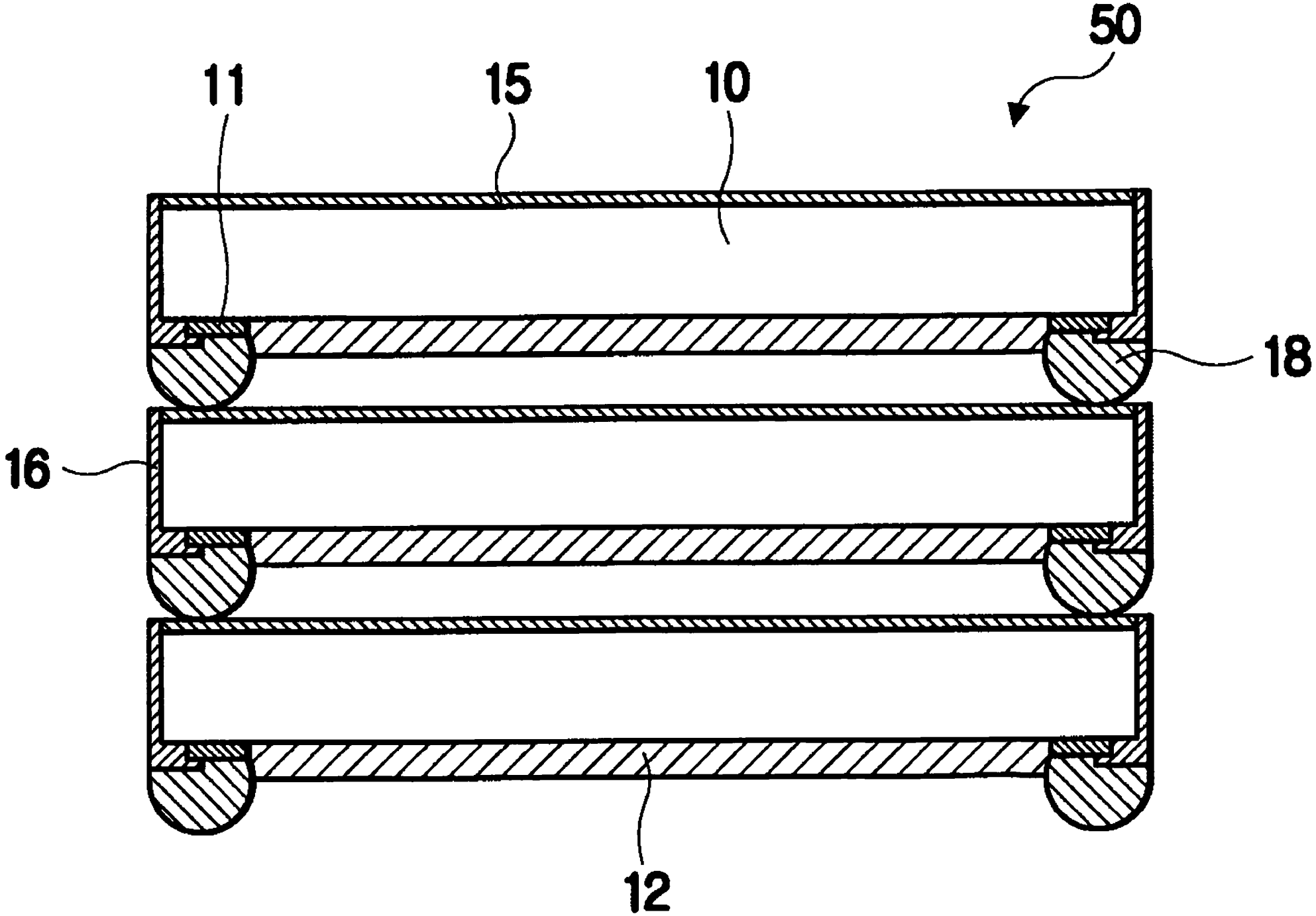
Abstract of **KR20010018694**

PURPOSE: A method for manufacturing a three-dimensional stacked chip package is provided to simplify a manufacturing process, by electrically interconnecting semiconductor chips located in upper and lower portions not in a stacked state of the semiconductor chips but in a wafer state.
CONSTITUTION: A passivation layer(12) is formed on an active surface of a wafer having a predetermined integrated circuit and electrode pad(11), to cover the integrated circuit and the electrode pad. Holes penetrating the wafer are formed along a scribe line to divide the wafer into individual unit semiconductor chips(10). A circuit pattern(15) adjacent to the holes is formed on a surface opposite to the active surface of the wafer. The electrode pad has an opened portion to eliminate the passivation layer from the holes to the electrode pad. A metal layer(16) in contact with the electrode pad and the circuit pattern is formed. An external terminal is formed on the electrode pad, projected from the passivation layer by a predetermined height. The scribe line is cut to separate the unit semiconductor chips from the wafer. The external terminal of the semiconductor chip located in an upper portion and the circuit pattern of the semiconductor chip located in a lower portion are connected to stack at least the two unit semiconductor chips.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